Method and the Computer System for Reducing the Possibility of Cold Reset

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BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a method and computer system for reducing the possibility of cold reset, and more particularly to a method and computer system that can prevent the lost of data stored in the synchronous dynamic random access memory (SDRAM) caused by battery faults so as to reduce the possibility of cold reset.

Description of the Related Art

[0002] For a computer system that relies on a battery as its main source of power supply, the computer system has to enter the sleep mode in order to reduce power consumption when a battery fault occurs. The battery fault means that when the battery is in low power or when the battery is detached from the computer system when the computer system experiences external impact and therefore the battery could not supply power anymore. Example

for the referred computer system could be a personal digital assistant (PDA).

[0003] Generally speaking, the central processing unit (CPU) used in a computer system has two modes: the normal operation mode and the sleep mode. If the CPU has the ability to handle battery fault, the CPU enter sleep mode directly when a battery fault occurs. But if the CPU supports the function of software battery fault handling, the CPU receives a battery fault indication event when a battery fault occurs. At this time, the battery fault indication event is regarded as an interrupt source. The interrupt source needs to be processed by software code before the CPU can enter the sleep mode.

[0004] After the CPU has entered the sleep mode when a battery fault had occurred, the remaining power, which includes the power stored in the equivalent capacitors and the power from a backup power supply, in the main circuit board of the computer system can carry on supplying power to the SDRAM in order to retain the data stored in the SDRAM. When a new battery or the detached battery is reinstalled properly by the user, the CPU can again be awakened and the status of the computer system can be restored back to what it was before the sleep mode, so that the user can continue to use the computer system. After the CPU is awakened, it has to execute hardware initialization before it can run application programs.

During the hardware initialization, software codes, which include boot code, are loaded.

[0005] However, if the CPU supports the function of software battery fault handling, the software code can handle the battery fault indication event, which can tell the CPU to enter the sleep mode, only after the hardware initialization is successfully completed by the CPU. If the battery fault occurs during the hardware initialization, the software code cannot handle the battery fault indication event, and therefore CPU can not enter the sleep mode. Consequently, the CPU has to stay in the normal operation mode, which consumes a great amount of power. Because no power supplied from the battery, the remaining power will be used up quickly. At this time, the data stored in the SDRAM will be lost completely because the main circuit board fails to supply power to the SDRAM. Data of the user and downloaded programs will be all erased. After the user has replaced the battery or has reinstalled the battery, the computer system can only proceed with cold reset that brings the system back to its default factory status because all the previous data in the SDRAM is lost.

[0006] For the sake of explanation, the period during which the CPU is executing hardware initialization is defined as the first period T1, and the period that the CPU can start running application programs is defined as the

second period T2.

[0007] Referring to FIG. 1, the timing diagram of the signals when a battery fault occurs during the first period T1 is shown. The power enable signal PWR_EN indicates whether the sleep mode is activated. When the power enable signal PWR_EN is enabled, for example with high voltage, the CPU is in the normal operation mode; whereas the CPU is in the sleep mode when the power enable signal PWR_EN is disabled. The CPU core power signal CPU_CR_PWR indicates the status of power supply for the core power of the CPU. When the CPU is in normal operation mode, the battery supplies power to the CPU normally, and therefore the CPU core power signal CPU_CR_PWR is in high voltage. When the CPU is in sleep mode, the battery stops supplying power to the CPU, and therefore the CPU core power signal CPU_CR_PWR is in low voltage.

[0008] Furthermore, the CPU peripheral component power CPU_IO_PWR indicates the status of power supply for the CPU's peripheral components. No matter whether the CPU is in the normal operation mode or in the sleep mode, power is always supplied to the CPU's peripheral components, and therefore the CPU peripheral component power CPU_IO_PWR is always in high voltage. The battery fault signal BTRY_FLT indicates whether any battery faults occur. When the battery fault signal BTRY_FLT is enabled, it is

changed to low voltage.

[0009] As shown in FIG. 1, the CPU is awakened from the sleep mode at the point t1, then the battery enable signal PWR_EN is changed to high voltage and the CPU enters the first period T1. If any battery fault occurs in the first period T1, a battery fault indication event 102 is generated and the battery fault signal BRTY_FLT is changed to low voltage. At this moment, the software code cannot handle the battery fault, and therefore the CPU keeps working in the normal operation mode in which great amount of power is consumed continuously. At point t2, because all the power in the main circuit board is used up, the main circuit board no longer supplies power to the SDRAM. Data stored in the SDRAM is therefore lost completely.

[0010] Refer to FIG. 2, the timing diagram of the signals when a battery fault occurs during the second period T2 is shown. When a battery fault occurs at the time point t3 in the second period T2, a battery fault indication event 202 is generated, the software code can successfully handle the battery fault indication event 202, and therefore the CPU can successfully enter the sleep mode in order to reduce power consumption. At this moment, the remaining power in the main circuit board can continue supplying power to the SDRAM so the data stored in the SDRAM can be safely preserved.

[0011] Therefore, the question of how to handle the battery fault, which happens in the first period, causing the remaining power in the main circuit board to be used up because the CPU is still in the normal operation mode and subsequently loses the data stored in the SDRAM because the main circuit board can no longer supply power to the SDRAM, is one of the research direction of the industry in order to reduce the possibility of cold reset.

SUMMARY OF THE INVENTION

[0012] It is therefore an object of the invention to provide a method and computer system for reducing the possibility of cold reset for computer systems. The invention can effectively prevent the problem of battery faults, which occurs in the first period causing data lost in the SDRAM, and also can reduce the possibility of cold reset.

[0013] The invention achieves the above-identified objects by providing a method and computer system for reducing the possibility of cold reset for computer systems. The computer system has a CPU that is used to control the computer system, a wake-up button that is used to awaken the CPU from a sleep mode, and a battery that supplies power to the computer system. The CPU supports the function of software battery fault handling. The

method of the invention includes the procedures (1) When the CPU is in the sleep mode and the computer system's power supply is in an uncertain status, the CPU staying in the sleep mode even a wake-up event occurs. (2) When the CPU is in the sleep mode and the period during which the wake-up button is pressed is less than a predetermined value, the CPU continues to stay in the sleep mode.

[0014] Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 shows the timing diagram of the signals when a battery fault occurs during the first period T1.

[0016] FIG. 2 shows the timing diagram of the signals when a battery fault occurs during the second period T2.

[0017] FIG. 3 shows a block diagram of a computer system for the above-identified procedure (1) of the method provided in a preferred embodiment of the invention.

[0018] FIG. 4A shows the timing diagram of the first signal S1 and the second signal S2when the CPU of FIG. 3 is in the sleep mode and the detection circuit 306 has determined that the computer system is in a status of uncertain power supply.

[0019] FIG. 4B shows the timing diagram of the first signal S1 and the second signal S2when the CPU of FIG. 3 is in the sleep mode and the detection circuit has determined that the computer system is not in a status of uncertain power supply.

[0020] FIG. 5 is a block diagram of a computer system for the above-identified procedure (2) of the method provided in a preferred embodiment of the invention.

[0021] FIG. 6A shown the timing diagram of the third signal S3 and the forth signal S4when the CPU in FIG. 5 is in the sleep mode and the period during which the wake-up button is pressed is less than the P value.

[0022] FIG. 6B shows the timing diagram of the third signal S3 and the forth signal S4when the CPU in FIG. 5 is in the sleep mode and the period during which the wake-up button is pressed is greater than the P value.

DETAILED DESCRIPTION OF THE INVENTION

[0023] The invention solves the problem of losing data stored in the SDRAM by preventing the occurrence of battery faults in the first period T1. The procedures provided by the method of the invention to prevent the occurrence of battery faults in the first period T1 include: (1) When the computer is in sleep mode and the computer system's power supply is in an uncertain status, wake-up events, if any of them occur, are not send to the CPU and therefore the CPU can stay in the sleep mode. (2) When the computer system is in the sleep mode, it determines whether the wake-up button is pressed accidentally by external impact according to the period during which the wake-up button is pressed. If the period during which the wake-up button is pressed is less than a predetermined value, the CPU continues to stay in the sleep mode. Procedure (1) and procedure (2) can be implemented together or implemented individually.

[0024] Please refer to FIG. 3, it is a block diagram of a computer system 300 for a preferred embodiment of the procedure (1) mentioned above. The computer system 300 includes a central processing unit (CPU) 302, a circuit unit 304, a detection circuit 306, and a battery 308. The CPU 302 is used to control the computer system 300, and it supports the function of software battery fault handling. The circuit unit 304 is electrically connected to the

CPU 302. The circuit unit 304 is used to receive a first signal S1 and output a second signal S2. The detection circuit 306 controls the circuit unit 304 according to the status of the computer system 300. And the battery 308 supplies power to the computer system 300.

[0025] Please refer to FIG. 4A, it is the first signal S1's and the second signal S2's timing diagram showing that the CPU 302 of FIG. 3 is in the sleep mode and the detection circuit 306 has determined that the computer system 300 is in a status of uncertain power supply. Assume that when the first signal S1 is enabled, the first signal S1 is in low voltage, and similarly for the second signal S2. When a wake-up event 410 occurs at the time point t4, the first signal S1 is changed to low voltage. When the CPU 302 is in the sleep mode and the detection circuit 306 has detected that the computer system 300 is in a status of uncertain power supply, the circuit unit 304 does not pass the wake-up event 410 to the CPU 302, and therefore the second signal S2 stays in high voltage. Even the wake-up event 410 has already been inputted into the circuit unit 304, because the CPU 302 does not receive the wake-up event, the CPU 302 remains in the sleep mode.

[0026] Refer to FIG. 4B, the timing diagram of the first signal S1 and the second signal S2 is shown when the CPU 302 of FIG. 3 is in the sleep mode and the detection circuit 306 has determined that the computer system 300 is

not in a status of uncertain power supply. When a wake-up event 420 occurs at the time point t5, the first signal S1 is changed to low voltage. When the CPU 302 is in the sleep mode, and the detection circuit 306 has determined that the computer system 300 is not in a status of uncertain power supply, then the circuit unit 304 passes the wake-up event 422 to the CPU 302. The CPU 302 is awakened.

[0027] When the computer system is in a status of uncertain power supply, the invention prevents the situation, in which the CPU 302 is awakened and subsequently enters the first period during which the hardware initialisation occurs, by not allowing the wake-up event to reach the CPU 302. This is because (I) if the computer system 300 is in (i) the battery fault status, in which the battery could not normally supply power, due to the reasons of the battery being flat or the battery being detached; or (ii) the status when the user opens the battery lid, which is used to immobilize the battery, in order to replace the battery; or (iii) the low power status when the battery's power level is too low, and (II) if the computer system 300 is awakened so that it starts the normal operation mode and enters the first period T1, during which hardware initialisation is carried out, then the battery is unable to supply power and subsequently the remaining power in the main circuit board is used up quickly causing the lost of data stored in the SDRAM. The invention allows the CPU

302 to stay in the sleep mode when the computer system is in any of the three statuses mentioned above by detecting the status of the computer system 300. Therefore, the CPU 302 will not enter the first period T1, and the problem, which is caused by the software code being unable to handle battery fault events in the traditional method, can be prevented. The remaining power in the main circuit board can continue to supply power to the SDRAM in order to preserve the data stored in the SDRAM. Therefore, the computer system 300 provided by the invention can prevent the lost of data in the SDRAM and can also reduce the possibility of cold reset.

[0028] Refer to FIG. 5, a block diagram of a computer system 500 that follows the procedure (2) mentioned above for a preferred embodiment of the invention is shown. The computer system 500 includes a wake-up button 530, a CPU 502, a delay protection circuit 532, and a battery 508. The wake-up button 530 is located on the external case of the computer system 500 for user's operation of the computer system. The CPU 502 is used to control the computer system 500, and it supports the function of software battery fault handling. The wake-up button 530 is applied for outputting a third signal S3 to the delay protection circuit 532, and the delay protection circuit 532 is applied for outputting a forth signal S4 to the CPU 502. The battery 508 supplies the power required by the computer system 500.

[0029] The wake-up button 530 can be pressed by a user's finger or by the impact when the computer system 500 falls to the ground. When the computer system 500 falls, it is possible that the battery is detached by the impact. Generally speaking, the period during which the wake-up button 530 is pressed due to a collision or an impact is about 1~2 millisecond, whereas the period during which the wake-up button is pressed by the user's finger is usually about 100 millisecond. Therefore, a predetermined value P, which has a default value of greater than 1~2 millisecond and less than 100 millisecond, is proposed in the invention, so that whether the wake-up button 530 is pressed intentionally or accidentally can be determined by checking the period during which the wake-up button 530 is pressed being less or larger than the value of P.

[0030] When the computer system 500 falls to the ground, the battery 508 may be detached. If the battery 508 is detached, the battery 508 cannot supply power to the computer system 500. At this moment, if the CPU 502 is awakened from the sleep mode, then the remaining power in the main circuit board will be used up quickly causing the lost of data stored in the SDRAM. Therefore, when the CPU 502 is in the sleep mode and the delay protection circuit 532 has detected that the period during which the wake-up button 530 is pressed is less than the P value, it means that the computer

system may have experienced a collision or an impact and the battery 508 may already has been detached. At this moment, the invention allows the CPU 502 to stay in the sleep mode to prevent the lost of data in the SDRAM.

[0031] Referring to FIG. 6A, timing diagram of the third signal S3 and the forth signal S4 is shown when the CPU 502 is in the sleep mode and the period during which the wake-up button is pressed is less than the P value. Assume that when the third signal S3 is enabled, it is in low voltage, and similarly for the forth signal S4. When a wake-up event 610 occurs at the time point t6, the third signal S3 is changed to low voltage. When the CPU 502 is in the sleep mode, and the delay protection circuit 532 has detected that the period during which the wake-up button 530 is pressed is less than the P value, the delay protection circuit 532, even it has received the wake-up event 610, does not send any wake-up event to the CPU 502. Therefore, the forth signal S4 outputted by the delay protection circuit 532 at the time point t6 still stays in high voltage, and the CPU still stays in the sleep mode.

[0032] Please refer to FIG. 6B, timing diagram of the third signal S3 and the forth signal S4 is shown when the CPU 502 of FIG. 5 is in the sleep mode and the period during which the wake-up button is pressed is greater than the P value. When a wake-up event 620 occurs at the time point t7, the third signal S3 is changed to low voltage. When the CPU 502 is in the sleep

mode, and the delay protection circuit 532 has detected that the period during which the wake-up button 530 is pressed is greater than the P value, it means that the user has pressed the wake-up button 530 and wants to awaken the computer system 500. Therefore, when the delay protection circuit 532 receives the wake-up event 620, the delay protection circuit 532 outputs a wake-up event 622 to the CPU 502. At this time, the forth signal S4 outputted by the delay protection circuit 532 is changed to low voltage at the time point t7, thus the CPU 502 is awakened.

[0033] The delay protection circuit 532 is controlled by a control signal CTRL. When the computer system 500 is in the sleep mode, the control signal CTRL is enabled and the delay protection circuit 532 is also enabled in order to execute the processes shown in FIG. 6A and FIG. 6B. But when the computer system 500 is in normal operation mode, the control signal CTRL is disabled and the delay protection circuit 532 is disabled. At this time, the third signal S3 can be directly pass to the CPU 502, and thereby the operational speed of the computer system 500 in the normal operation mode is increased.

[0034] The method and computer system for reducing the possibility of cold reset provided by the invention can effectively prevent battery faults, which causes the problem of losing data in the SDRAM, from happening

during the first period T1. The invention provides the advantage of improved data completeness and increased length of time during which data can be stored in the SDRAM for computer systems especially for PDAs.

[0035] While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.